

LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-11: Canceled.

12. (Previously Added) A semiconductor device comprising:

a lead frame, said lead frame including a conductive die pad having a first major surface and a second major surface opposing said first major surface, and a first plurality of leads disposed at a first edge of said conductive die pad and a second plurality of leads disposed at a second edge of said conductive die pad, said second edge of said conductive die pad being opposite to said first edge of said conductive die pad;

a first semiconductor die having a first major electrode of a first functionality disposed on a first major surface thereof, and a second major electrode of a second functionality disposed on a second opposing major surface thereof, said first major electrode of said first semiconductor die being electrically connected to said first major surface of said conductive die pad;

a second semiconductor die having a first major electrode of a first functionality disposed on a first major surface thereof, and a second major electrode of a second functionality disposed on a second opposing major surface thereof, said first major electrode of said second semiconductor die being electrically connected to said second major surface of said conductive die pad; and

a molded housing encapsulating said conductive die pad, said first semiconductor die, said second semiconductor die, and portions of said first plurality of leads and said second plurality of lead;

wherein said second major electrode of said first semiconductor die and said second major electrode of said second semiconductor die are electrically connected to said first plurality of leads and said conductive die pad is electrically connected to at least one of said second plurality of leads, whereby said first major electrode of said first semiconductor die and said first major electrode of said second semiconductor die are electrically connected to one another and to said at least one of said second plurality of leads.

13. (Previously Added) A semiconductor device according to claim 12, wherein at least one of said semiconductor die is a MOSFET.

14. (Previously Added) A semiconductor device according to claim 12, wherein said first semiconductor die includes a control electrode on said second major surface thereof, and said second semiconductor die includes a control electrode on said second major surface thereof.

15. (Previously Added) A semiconductor device according to claim 12, wherein said first plurality of leads include four spaced leads, and said second plurality of leads include four spaced leads.

16. (Previously Added) A semiconductor device according to claim 12, wherein said first major electrode is a drain electrode of a MOSFET die and said second major electrode is a source electrode of a MOSFET die.

17. (Currently Amended) A semiconductor die according to claim 14, wherein each of said semiconductor die is a MOSFET, said control electrode is a gate electrode, said first major electrode is a drain electrode, and said second major electrode is a source electrode, and wherein said gate electrodes of said MOSFETs are electrically connected to one of said plurality of second leads, said source electrodes of said MOSFETs are electrically connected to another one of said second plurality of leads, and said conductive die pad is electrically connected to the remaining leads of said second plurality of leads, and said source electrodes of said ~~MOSFETS~~ MOSFETs are also connected to said first plurality of leads.

18. (Previously Added) A semiconductor device according to claim 17, wherein all electrical connections are made by wires.

19. (Previously Added) A semiconductor device according to claim 12, wherein said first plurality of leads are spaced from said conductive die pad and said second plurality of leads are spaced from said conductive die pad.